IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application	:	Petrus Maria De Greef
For	:	DISPLAYING ON A MATRIX DISPLAY
Serial No.	:	10/587,604
Filed	:	July 27, 2006
Art Unit	:	2628
Examiner	:	Edward Martello
Atty. Docket	:	NL040106US1
Confirmation No.	:	3561

APPEAL BRIEF

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P.O. Box 1450
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Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed previously.

I. REAL PARTY IN INTEREST

The party in interest is NXP B.V., by way of an Assignment recorded at Reel 019719, frame 0843.

II. RELATED APPEALS AND INTERFERENCES

Following are identified any prior or pending appeals, interferences or judicial proceedings, known to Appellant, Appellant's representative, or the Assignee, that may be related to, or which will directly affect or be directly affected by or have a bearing upon the Board's decision in the pending appeal:

Appeal Brief Filed March 18, 2009.

III. STATUS OF CLAIMS

Claims 1-11 are on appeal.

Claims 1-11 are pending.

No claims are allowed.

Claims 1-11 are rejected.

No claims are canceled.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The subject matter recited in claim 1 relates to a method of displaying an image comprising the steps of: storing the source data in a frame memory under control of a first address pointer having a start address being determined by the source frame synchronization instants (see Figs. 1 & 2; page 4, lines 18-24), reading

during a read period display data from the memory under control of a second address pointer having a start address being determined by display frame synchronization instants having a display frame rate (see page 4, lines 34-39), displaying the display data on a matrix display (see page 3, lines 34-36), and controlling the source frame rate or the display frame rate to obtain, in a stable situation, the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period and a ratio of two between the display frame rate and the source frame rate (see Figs. 3 & 5; page 5, lines 9-23).

The subject matter recited in claim 2 relates to a system of displaying an image (see figs. 1 & 2), comprising: a video source (see page 3, lines 24-28) for generating images comprising source data and source frame synchronization instants having a source frame rate, means (see page 3, lines 18-24) for storing the source data in a frame memory under control of a first address pointer having a start address being determined by the source frame synchronization instants, means (see page 4, lines 34-39) for reading during a read period display data from the memory under control of a second address pointer having a start address being determined by display frame synchronization instants having a display frame rate, means (see page 3, lines 35-37) for displaying the display data on a matrix display and means (see figs. 3 & 5; page 5, lines 9-23) for controlling the source frame rate or the display frame rate to obtain, in a stable situation, the first address pointer and the second address pointer starting with an offset in time which has a fixed

polarity during the read period and a ratio of two between the display frame rate and the source frame rate.

The subject matter recited in claim 5 relates to a system of displaying an image as claimed in claim 4, wherein the means for adapting are arranged to obtain the offset in time between the first pointer and the second pointer being substantially equal to half a source write period, the source write period being the period in time required for the storing of the source data of one source frame of the source data (see figs. 3 & 5; page 2, lines 53-56).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are presented for review:

A. Claims 1-8 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over European Patent Application Publication EP 0875882 to Schiefer et al. (hereinafter "Schiefer").

B. Claims 9-11 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Schiefer in view of U.S. Patent Application No. 2003/0164897 to Chen et al. (hereinafter "Chen").

VII. ARGUMENTS

A. Rejection of Claims 1-8 Under 35 U.S.C. § 103

The Final Office Action dated June 11, 2009, rejects claims 1-8 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Schiefer. Applicant respectfully traverses this rejection.

The United States does not grant patents for inventions that would have been obvious to a person of ordinary skill in the art at the time of the invention. 35 U.S.C. § 103 (2000); MPEP § 2142. In an obviousness inquiry, the court determines 1) the scope and content of the prior art; 2) the differences between the claimed invention and the prior art; 3) the level of ordinary skill in the art; and 4) secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 1718 (1966). An invention that otherwise might be viewed as an obvious modification of prior art will not be deemed obvious when a prior art reference teaches away from the invention. *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1354 (Fed. Cir. 2000).

1. Claims 1 & 2

Independent claim 1 recites, in part, "A display method comprising . . . controlling the source frame rate or the display frame rate to obtain, in a stable situation, the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period and a ratio of two between the display frame rate and the source frame rate (emphasis added). Independent claim 2 contains similar recitations.

As described in the specification in paragraph [0009], this subject matter relates to the use of a controller to control both the read and write address pointers in the memory that uses a single circular buffer in order to prevent video tearing. When the source and display frame rates are not equal, the controller adjusts both the frame rates and the address pointers so that, during the read period, one pointer does not cross the other, thus preventing tearing. *See* ¶ [0015], [0063]. Such adjustments have advantages, such as lowering the required source frame rate, lower power consumption, and reduce flickering. *See* ¶ [0063]. This is highlighted by three features: (1) a time offset between the two address pointers, (2) a fixed polarity of the pointers during the read period, and (3) a constant ratio between the display frame rate and the source frame rate (here, the ratio is equal to 2). *See* ¶ [0054].

In contrast, Schiefer fails to disclose, teach, or suggest "controlling means for controlling the source frame rate or the display frame rate to obtain the address pointers, where the pointers start with a time offset, there is a fixed polarity between the pointers, and there is a ratio of two between the display and source frame rates," as recited in claim 1 and similarly recited in claim 2. Schiefer discloses a timing generator for format conversion of video. *See Abstract.* This system reformats video by *synchronizing* the output and input frame rates, using a memory buffer in case of errors to ensure a smooth display. The memory write controller controls write operations sequentially in a circular buffer sequence. *See col. 13, lns. 34-39.* The data path, once full, is then controlled by a timing controller.

In section 19 on page 12, the Office Action states that Schiefer "points to the detailed timing diagrams of the data buffering section of the invention where it is shown that the **output write clock is running at rate of four times the input clock rate** in the example given" (emphasis in original). As this timing diagram of the *clock rates* indicates, Schiefer substantially differs in operation from the recited subject matter.

The recited subject matter recites a ratio of two between the display frame rate and the source frame rate, as the single circular buffer allows *at maximum*, a ratio of 2 (1:2 or 2:1) between the respective frame rates to function properly without any video tearing. *See e.g., Figs. 5A-5E, ¶¶ [0061]-[0063].* The ratio of 4:1 disclosed by Scheifer and cited by the Examiner as the ratio between the respective address pointers in the singular buffer would guarantee video tearing, as one pointer with a rate four times faster than the other would always overtake the other pointer during at some point in the circular buffer and would do so multiple times during a single traversal of the slower pointer through the circular buffer.

Furthermore, Schiefer discloses a system that scales and deinterlaces the input video and *matches the frame rate* of the input video with that of the output. The large ratio between input and output *clock rates* ("DCLK = 4*IPCLK", *see Fig. 11*) disclosed by Schiefer and cited by the Examiner **does not** relate the ratio between the *input and output frame rates* recited by the above subject matter. Rather, the 4:1 ratio discussed in the Schiefer specification relates to the system horizontally and vertically upscaling an input image by a factor of 2 for an output

video, while maintaining the locked, similar frame rate through the control of the respective *line rates*, (*see col. 21, lns. 15-33* (discussing display line rate as a fractional multiple of the input video main clock)). These line rates differ due to the respective number of pixels per line in the input and output images. *See, col. 21, lns. 34-46* (discussing means to force frame locking so the resulting display frame period is similar to the input video frame period.)

A person of ordinary skill in the art, therefore, would not refer to Schiefer, which discloses a solution for scaling a video image using a 4:1 clock ratio for line rates, to create the recited subject matter, which has a maximum working limit of 2:1 between frame rates, as Schiefer's disclosure would make the recited subject matter unusable. The Examiner has used impermissible hindsight to conclude that a person of ordinary skill in the art would refer to a device that explicitly discloses an unworkable range between variables in order to create the recited subject matter. Therefore, Schiefer does not disclose, teach, or suggest, "controlling the source frame rate or display frame rate to obtain . . . a ratio of two between the source frame rate and the display frame rate," as recited in independent claim 1 and similarly recited in independent claim 2.

In addition, while Schiefer does disclose a half-line offset, Schiefer discloses a half-line offset "to maintain a constant period between lock events" with the source and output *having the same frame rates*, with the offset time used to minimize timing errors. *See col. 17, lns. 17-20.* This motivation is different from the recited subject matter, which uses a half-line offset to allow the system to properly *support*

differing frame rates, to a maximum of a 2:1 ratio. Schiefer, therefore, does not disclose, teach, or suggest an offset to support a non-identical ratio between input and output frame rates, nor does Schiefer disclose, teach, or suggest *any support* of a non-identical ratio of two between the display frame rate and the source frame rate. *See, e.g., col. 21, lns. 34-46.*

As such, Schiefer fails to disclose, teach, or suggest to a person of ordinary skill in the art all the elements recited in claims 1 and 2. Schiefer therefore does not render claims 1 and 2 obvious.

2. Claims 3-8

Claims 3-8 depend on claim 2 and are therefore also allowable for at least the reasons detailed above in connection with independent claims 1 and 2, as well as for the separately patentable subject matter recited therein.

B. Rejection of Claims 9-11 Under 35 U.S.C. § 103

The Final Office Action dated June 11, 2009, rejects claims 9-11 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Schiefer in view of Chen. Applicant respectfully traverses these rejections.

Claims 9-11 depend from independent claim 2. Chen discloses a system to prevent buffer over- or under-flow, with the input and output rates being equal. *See Abstract.* Chen also discloses a display frame period being the inverse of the display frame rate and controlling the display frame rate by adjusting the idle time (time

between read periods). Chen therefore fails to overcome the deficiencies of Schiefer described above in connection with independent claim 2.

Claims 9-11 are therefore patentable for at least the reasons stated above in connection with claim 2, as well as for the separately patentable subject matter recited therein.

C. Conclusion

For at least the reasons discussed above, it is respectfully submitted that the rejections are in error and that claims 1-11 are in condition for allowance. For at least the above reasons, Appellants respectfully request that this Honorable Board reverse the rejections of claims 1-11.

In the event that the fees submitted prove to be insufficient in connection with the filing of this paper, please charge our Deposit Account Number 50-0578 and please credit any excess fees to such Deposit Account. Should there be any remaining issues that could be readily addressed over the telephone; the Examiner is asked to contact the attorney overseeing the application file, Aaron Waxler, of NXP Corporation at (408) 474-5256.

Respectfully submitted,
KRAMER & AMADO, P.C.

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Date

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VIII. CLAIMS APPENDIX

CLAIMS INVOLVED IN THE APPEAL:

1. (Previously Presented) A display method comprising:

generating images comprising source data and source frame synchronization instants having a source frame rate,

storing the source data in a frame memory under control of a first address pointer having a start address being determined by the source frame synchronization instants,

reading during a read period display data from the memory under control of a second address pointer having a start address being determined by display frame synchronization instants having a display frame rate,

displaying the display data on a matrix display, and

controlling the source frame rate or the display frame rate to obtain, in a stable situation, the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period and a ratio of two between the display frame rate and the source frame rate.

2. (Previously Presented) A display system comprising:

a video source for generating images comprising source data and source frame synchronization instants having a source frame rate,

means for storing the source data in a frame memory under control of a first address pointer having a start address being determined by the source frame synchronization instants,

means for reading during a read period display data from the memory under control of a second address pointer having a start address being determined by display frame synchronization instants having a display frame rate,

means for displaying the display data on a matrix display and means for controlling the source frame rate or the display frame rate to obtain, in a stable situation, the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period and a ratio of two between the display frame rate and the source frame rate.

3. (Previously Presented) A display system as claimed in claim 2, wherein the means for controlling comprise:

means for comparing the source frame synchronization instants and the display synchronization instants or signals related thereto, and

means for adapting the source frame rate or the display frame rate in response to the comparing to obtain the second pointer always lagging the first pointer during the read period in times or the other way around.

4. (Previously Presented) A display system claimed in claim 2, wherein the means for controlling comprise:

means for determining the offset in time between one of the source frame synchronization instants and one of the display frame synchronization instants succeeding each other, and

means for adapting the source frame rate or the display frame rate to obtain a substantially identical source frame rate and display frame rate and a predetermined fixed value of the offset in time.

5. (Previously Presented) A display system as claimed in claim 4, wherein the means for adapting are arranged to obtain the offset in time between the first pointer and the second pointer being substantially equal to half a source write period, the source write period being the period in time required for the storing of the source data of one source frame of the source data.

6. (Previously Presented) A display system as claimed in claim 2, wherein the means for displaying the display data further comprise:

means for generating a clock signal, and means for generating the display frame synchronization instants using the clock signal, and wherein

the means for controlling the display frame rate comprise means for adapting a frequency of the clock signal.

7. (Previously Presented) A display system as claimed in claim 2, wherein the means for displaying the display data further comprise:

means for generating a clock signal, means for generating line instants indicating a start of the lines of the display data using the clock signal, the line instants determining line periods, and

means for generating the display frame synchronization instants using the line instants, and wherein

the means for controlling the display frame rate comprise means for adapting a frequency of the clock signal to vary a duration of the line periods.

8. (Previously Presented) A display system as claimed in claim 2, wherein the means for displaying the display data further comprise:

means for generating a clock signal, means for generating line instants indicating a start of the lines of the display data by counting the clock signal, the line instants determining line periods, and

means for generating the display frame synchronization instants using the line instants, and wherein

the means for controlling the display frame rate comprise means for adapting a frequency of the clock signal to vary a duration of the line periods.

9. (Previously Presented) A display system method as claimed in claim 2, wherein a display frame period has a duration being an inverse of the display frame rate and comprises the means for the read period and an idle period,

wherein during the read period, the means for reading are arranged for reading the display data from the memory under control of the second address pointer, and

wherein during the idle period no display data is read from the memory and wherein the means for controlling the display frame rate comprises means for varying the idle time.

10. (Previously Presented) A display system as claimed in claim 2, wherein the means for controlling comprise:

means for determining the offset in time, and

means for adapting the display frame rate to obtain a display frame rate being substantially identical to two times the source frame rate and to obtain a predetermined fixed offset in time, by having

(i) the second pointer pointing to a first source video line of an already stored source video frame at an instant preceding the instant the first pointer is pointing to a first source video line a next source video frame to read the first source video line before the first source video line of the next source video frame is stored, and

(ii) the second pointer pointing to a last source video line of the next source video frame at an instant later than an instant the first pointer is pointing to the last source video line of the next source video frame to read the last source video line of the next source video frame after it has been stored.

11. (Previously Presented) A display system as claimed in claim 2, wherein a display frame period has a duration being an inverse of the display frame rate and comprises the read period and an idle period, wherein during the read period, the means for reading are arranged for reading the display data from the memory under control of the second address pointer, and wherein during the idle period no display data is read from memory and wherein the means for controlling comprise:

means for setting a free running display frame rate to a value lower than the value of the source display frame rate wherein a duration of the read period is shorter than a source frame period, and

means for restarting the display frame periods in response to received source synchronization instants.

IX. EVIDENCE APPENDIX

A copy of the following evidence 1) entered by the Examiner, including a statement setting forth where in the record the evidence was entered by the Examiner, 2) relied upon by the Appellant in the appeal, and/or 3) relied upon by the Examiner as to the grounds of rejection to be reviewed on appeal, is attached:

NONE

X. RELATED PROCEEDINGS APPENDIX

Following are identified any prior or pending appeals, interferences or judicial proceedings, known to Appellant, Appellant's representative, or the Assignee, that may be related to, or which will directly affect or be directly affected by or have a bearing upon the Board's decision in the pending appeal:

NONE